

High Density Packaging Technologies for RF Electronics in Small Spacecraft

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Abstract—This paper will describe a few high density packaging technologies which we are currently exploring for use in current and future small spacecraft applications. The three categories of technologies include organic multichip modules (MCMs), ceramic leadless surface mount technology (SMT) and 3D printed waveguide structures. There are many other packaging technologies that currently exist but these three were selected in part due to their long heritage in various commercial, military and space applications along with each having a relatively clear path to flight. For each of these technologies, detailed examples will be included in which hardware has been fabricated and tested for use in RF electronics for spacecraft transponders. The organic MCM example will be described in most detail and it utilizes a packaging technology by the name of CoreEZ which is a trademark of i3 Electronics. This MCM has shrunk a portion of our electronics down to 1/8th of its previous area. The CoreEZ technology has been shown to be rad hard beyond a total ionizing dose (TID) of 300kRad and the MCM which was fabricated has gone through thermal cycling and shown to have no degradation in performance. The ceramic leadless package examples include packages from high reliability manufactures by the name of KCB solutions and Barry Industries. In the case of KCB solutions, we have multiple products that will be described including a hermetic ceramic carrier which houses three microwave monolithic integrated circuits (MMICs) along with small discrete components. Finally, we will discuss the results of our search for a 3D printing process that allows us to reduce the cost and volume of our waveguide filters and diplexers for low cost small satellite applications. We have fabricated a few prototypes using direct metal laser sintering (DMLS) and metal coated plastics. Each of these packaging technology discussions will have a brief overview of its current and future use.

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1. INTRODUCTION

With the current trend in Cubesat and small satellite missions has come the need for further shrinking the size of existing spacecraft electronics. The spacecraft transponder is a necessary part of the spacecraft telecommunication system in which there are electronics that are especially sensitive to the effects of condensing hardware. Issues that arise when reducing the allocated volume include electromagnetic interference (EMI), poor thermal transfer and increased circuit parasitics. The radio frequency (RF) electronics typically operates at a higher frequency than that of the rest of the transponder. This high frequency signal has a shorter wavelength which makes it more susceptible to the effects of relatively small interconnect discontinuities and impurities in the surrounding materials which are supporting the transfer of the signal energy or electromagnetic wave. Due to the sensitive nature of the RF electronics and its corresponding signals, various RF circuits have been selected as candidates to determining the feasibility of a particular packaging technology.

There are three packaging technologies which will be discussed and they are as follows; organic MCMs, ceramic leadless carriers and 3D printed waveguide structures. For all of these categories, there is a portion of the transponder RF electronics which has been fabricated in order to give us some confidence that if it works for the RF, it should work for the digital and power electronics for at least in the difficult category of signal integrity.

2. ORGANIC MULTICHIP MODULES

MCM Technology Description

MCMs have been used for decades throughout the commercial market in an attempt to miniaturize printed circuit board assemblies. What allows this miniaturization is the ability of the MCM to support small interconnect feature sizes and thin dielectric laminates. Careful material selection and precise tooling must exist in order to assure the MCM can be reliably and repeatedly manufactured. The manufacturing process requires tooling that is more precise compared to those used in standard printed circuit board (PCB) fabrication. Ultraviolet (UV) Laser drilling for example, is commonly used throughout the process in order

to realize microvias that can be as small as 50 μ m in diameter. For these reasons a vendor that has experience with material handling and fabrication is essential in guaranteeing that the end product will be successfully delivered. In the case of our MCM demonstration we were fortunate enough to be able to work with i3 Electronics which is a company that spun off of IBMs packaging division in Endicott, New York. i3 Electronics has the manufacturing tools and experience necessary to perform the complete MCM fabrication from layout to final lid attach.

The first step in designing an MCM is selecting the packaging material and in the case of our prototype MCM, this was the CoreEZ material from i3 Electronics. The reason for selecting this material is that it has seen significant advancement and application in the aerospace and medical fields. There is a vast amount of radiation, electrical and reliability test results [1] for CoreEZ as published by i3 Electronics.

The CoreEZ dielectric material is composed of a P-Aramid thin core build-up and silica-filled high glass transition temperature (Tg) epoxy resin-coated copper [2]. The P-Aramid core improves the heat resistance and strength of the core while the high Tg prevents any softening of the adhesive bonding layers. The base interconnect metal for CoreEZ is copper with all of the exposed pads having a plating structure of 200 micro-inches of electrodeposited Nickel with a top layer of 4 micro-inches of gold. The interconnect mechanism to the carrier printed circuit board is primarily a ball grid array (BGA) style of solder balls which are coined to give them a flattened surface.

As a point of reference, for our CoreEZ MCM prototype we transferred the design from a PCB that was about 62 mils thick and approximately 8 metal layers to an MCM that supports 10 metal layers and is about 28 mils thick. The via diameter reduction went from about 10 mils minimum in the PCB down to 2 mils in the MCM. Along with via diameter and laminate thickness reduction is the ability to reduce the overall line width and line spacing in the MCM. For PCBs we typically do not like to go less than a 4 mil wide line with 4 mil spacing whereas for a CoreEZ MCM we can go down to just under 1 mil line widths and 1 mil line spacing when necessary.

In addition to the dielectric and metal interconnect support, CoreEZ also lends itself to accommodating the attachment of a lid. The lid is typically metal and can be a custom shape depending on the mechanical and thermal analysis of the package. The lid provides many benefits including improved thermal mass, mechanism for heat transfer, maintaining substrate flatness and providing EMI isolation within the package and from any outside electrical noise. The lid can be made of just about any material but for thermal reasons it is typically a gold over nickel plated copper. For die that are flip chip in which the heat escapes from the backside of the die, there is typically a thermal interface material between the backside of the die and the

underside of the lid. Figure 1 below shows a cross-section of a flip chip die on a CoreEZ substrate [4].

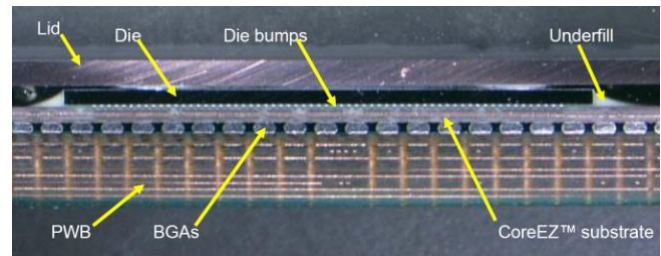


Figure 1. Cross section of flip chip device mounted to a CoreEZ substrate [4].

CoreEZ supports a variety of layer stack up configurations along with various die mounting assembly processes. The stack up which we utilized is known as a 3-4-3 buildup composed of 3 symmetric build-up layers on the top and bottom of the laminate and a 4 metal layer inner core which provides additional mechanical stability to the MCM. A cross-section of the 3-4-3 stack up is shown in Figure 2 below [3].

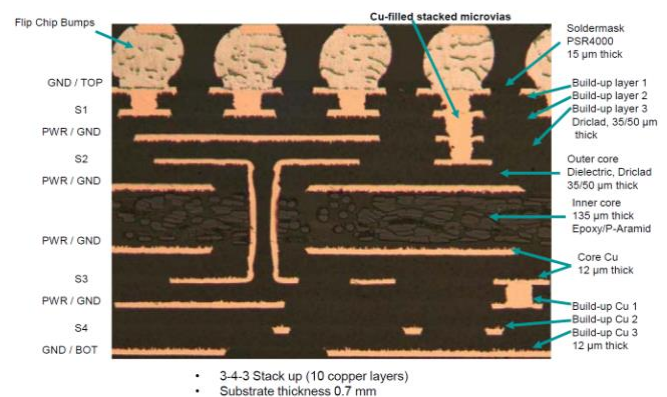


Figure 2. Cross section of 3-4-3 CoreEZ MCM with flip chip device mounted to top layer [3].

The die and device attach methods supported in the MCM include SMT, flip chip and wire-bond. We utilized all 3 of these methods in our MCM due to the die availability and a desire to show that i3 could reliably fabricate an MCM with various assembly methods. For all of the wire-bond parts, a mold compound or glob top encapsulation was placed over the wirebond region similar to that shown in the diagram of Figure 3 [5].

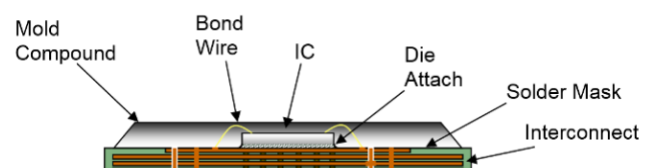


Figure 3. Diagram showing the IC with a mold compound in place to protect the die wire bond interconnections [5].

In order to minimize routing real estate, flip chip interconnections to all devices is the preferred method for die interface. In some cases where the backside of the die needs to be connected directly to a voltage or ground, we decided to wirebond the device and attach the die using an electrically conductive epoxy. For die where the backside of the die was a floating potential, i3 was able to solder bump the interconnection pads for flip chip attachment as shown in figure 4 below.

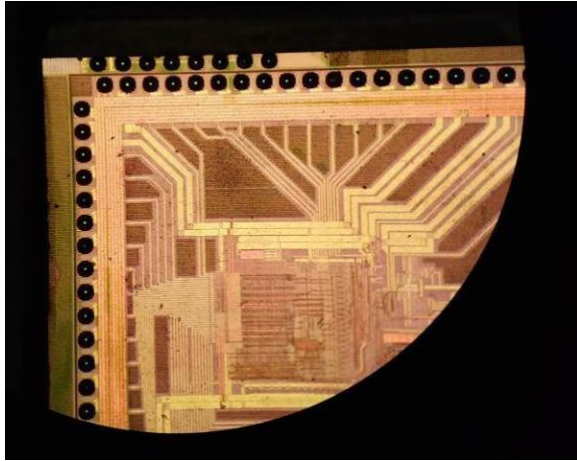


Figure 4. A microscope top view of a solder bumped integrated circuit.

In addition to wire bond and flip chip interconnection of devices, the other mechanism for attaching and interfacing to components was SMT. SMT attachment on the MCM is similar to that on a PCB where typically solder is used to attach terminals to the laminate metal plated pads. The solder used on the SMT parts should have a higher melting point than that of the BGA solder balls in order to avoid reflow of the SMT parts during the MCM attachment to the printed wiring assembly. One advantage of the MCM SMT attachment process is that it can accommodate smaller case sizes which wherever possible we used an 0201 case size. An 0201 case size implies a component such as a resistor, capacitor or an inductor which is 20 mils long by 10 mils wide. In the following section we will describe the MCM functionality and final implementation in more detail.

MCM Prototype Description

A necessary sub-circuit of the Transponder Exciter is the local oscillator (LO). The LO is used to generate the carrier which typically feeds a modulator where the carrier is modulated with digital waveforms. In addition to the Exciter, an LO is also used in the Transponder Receiver in order to generate a mixer tone which is used to down-convert the received RF signal to an intermediate frequency (IF). The IF is typically a low frequency signal that can be sampled via an analog to digital converter and then processed using digital signal processing. Due to the LOs relative complexity and frequent use, we chose this circuit to implement using the MCM. Typically the LO is realized

in the form of a phase locked loop (PLL) frequency synthesizer as shown in Figure 5.

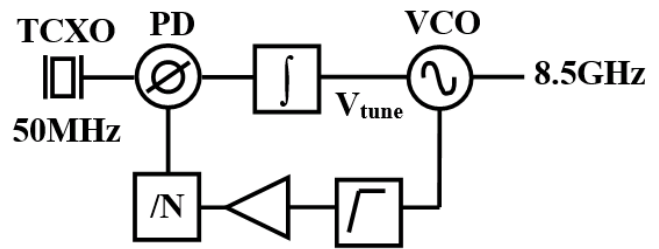


Figure 5. Block diagram of a PLL frequency synthesizer LO.

The PLL frequency synthesizer phase locks the VCO output frequency to the stable temperature compensated crystal oscillator (TCXO). At a high level the PLL behaves as a frequency multiplier in which the output signal maintains the phase noise characteristics of the TCXO within the loop bandwidth of the integrator and takes on the phase noise of the VCO outside of the integrator loop bandwidth. There are various devices required to realize a PLL. Specifically in the case of the ICs used in our PLL, there is also a variety of device assembly types. For example, the phase detector IC was modified to be attached using flip chip solder balls, the integrator utilizes a wire bonded op-amp and the VCO is a MMIC VCO which requires the bottom of the die to be attached to a ground pad and wire bonds attached to die top layer pads then terminated on the MCM pads. The final MCM was designed to accommodate all devices except for the TCXO and a photo of the final unpopulated MCM is shown from the top view in Figure 6.

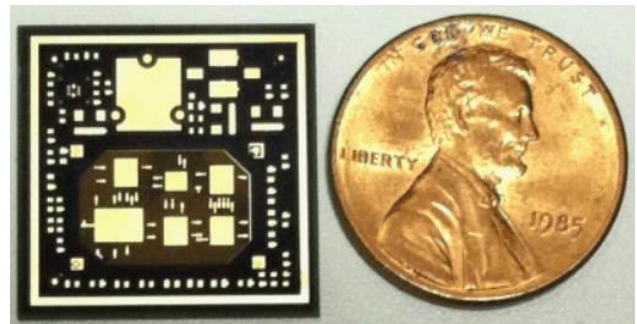


Figure 6. A top view of the final unpopulated PLL Frequency Synthesizer MCM.

The MCM measures approximately 19.5mm long by 19.5mm wide by 0.75mm thick and is less than 1/10th of the area required when using the commercial off the shelf (COTS) packaged versions of each device. The top and bottom views of the assembled MCM are shown in Figures 7 and 8 respectively.

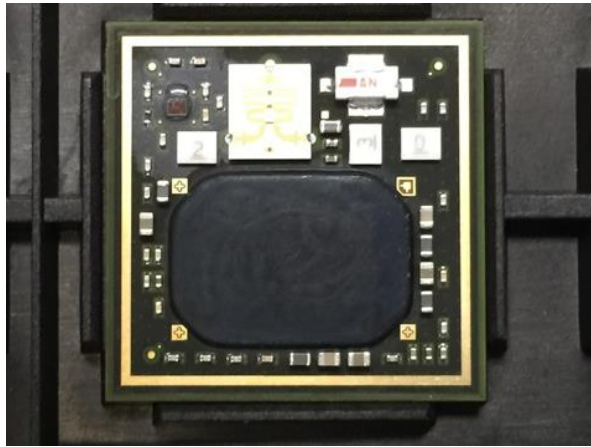


Figure 7. Top view of the final assembled PLL Frequency Synthesizer MCM.

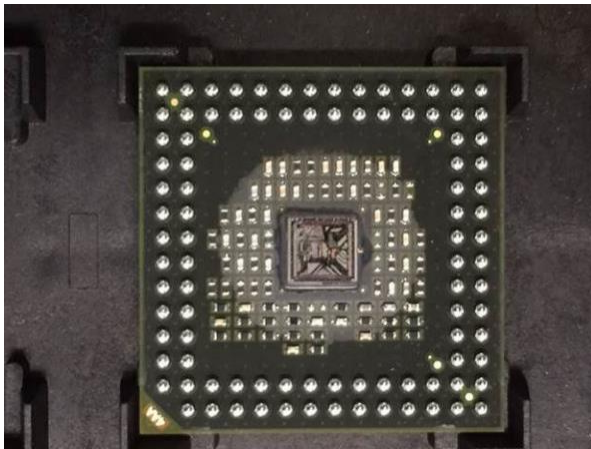


Figure 8. Bottom view of the final assembled PLL Frequency Synthesizer MCM.

Figure 7 shows the top view of the MCM in which all exposed parts are SMT attached and the devices underneath the glob top are wire-bonded parts. The glob top is used to protect the device wire-bonds and exposed die circuits. Also on the top layer is a small flip chipped device with thermal under-fill. The thermal under-fill is used as a barrier which absorbs the flip chip solder ball stress caused by coefficient of thermal expansion (CTE) mismatch between the silicon on sapphire die substrate and the MCM laminate. The bottom layer of the MCM has a flip chip PLL device with thermal under-fill, the BGA Snpb63 solder balls and SMT components. There are 95 BGA solder balls on the MCM along with close to 150 parts.

MCM Test Results

After fabrication and assembly, the fully assembled unlidded MCM was attached to a test board as shown in Figure 9 and Figure 10.

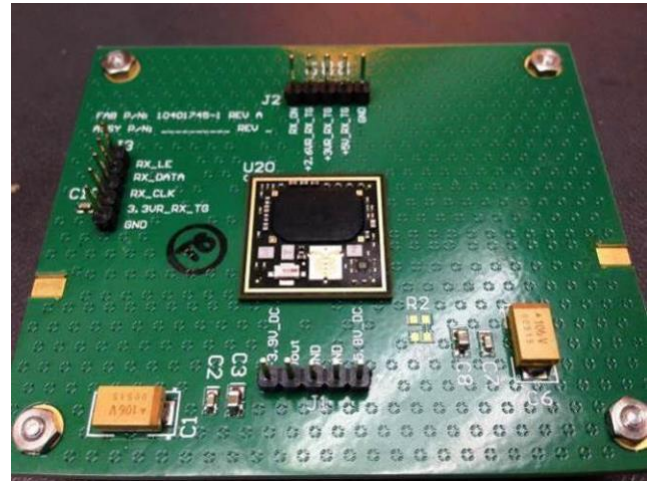


Figure 9. Top view of assembled MCM attached to test board.

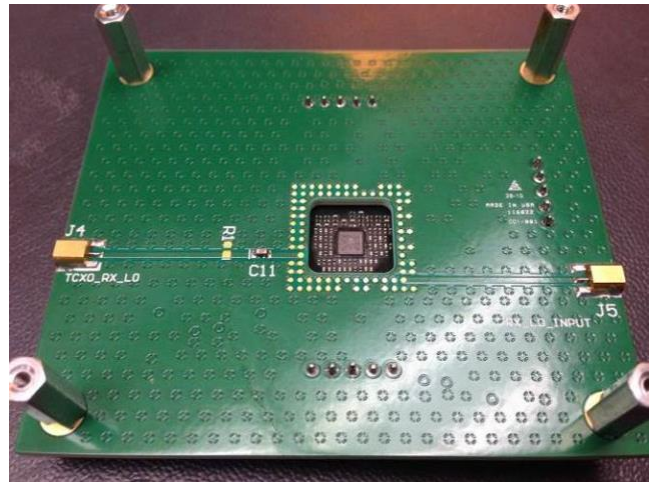


Figure 10. Bottom view of assembled MCM attached to test board.

In addition to the MCM, also attached to the test board are headers which provide test access points to the MCM, power to the MCM and a serial peripheral interface (SPI) for programming the PLL. There are also GPPO edge mount RF connectors for providing the TCXO input and an output for the LO. The MCM is attached to the test board similar to how a standard BGA part would be attached in that the solder balls are reflowed to the circular pads on the board. Figure 11 shows the MCM next to a gold colored CQFJ package which is the COTS packaged version of the PLL IC mounted flip chip on the bottom of the MCM. The COTS packaged PLL integrated circuit alone measures 24mm by 24mm by 3.3mm. From the photo one can see that this packaged IC alone is larger than the MCM.

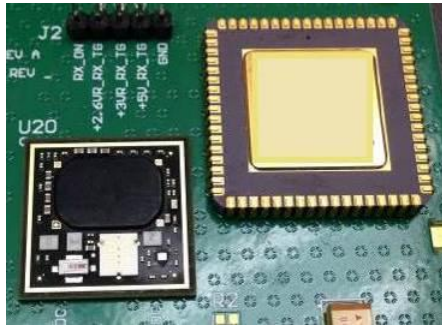


Figure 11. Top view of assembled MCM attached to test board next to the gold colored COTS packaged version of the PLL IC.

In cases where rad hard die were available, they were used for the MCM. All of the commercial die were verified to have a similar die that has a path to flight. An additional benefit of the MCM is that it allows us to allocate more volume to a radiation vault if a mission requires it.

The total DC power dissipation for the MCM was about 0.5W. Some of this DC power dissipation is due to the drop out required by the voltage regulators which are used to regulate the voltage levels to the devices and filter out noise from the main power supply and environment. Phase noise, spurious, output power and harmonics were some of the RF performance parameters which were measured. The total RF output power measured about 1mW, the spurious less than -60dBc, harmonics less than -25dBc and phase noise of -90dBc/Hz at 100 kHz offset with a loop bandwidth setting of about 100 kHz. A plot of the output phase noise is shown in figure 12 and the output spectrum in figure 13. The RF output power was a couple dB lower than expected and this may be due to losses in the package interconnects and transitions through the wirebonds and BGA. More MCMs would need to be tested or simulations performed in order to determine the final root cause of these added losses as they may also simply be due to the VCO part to part variation in output power.

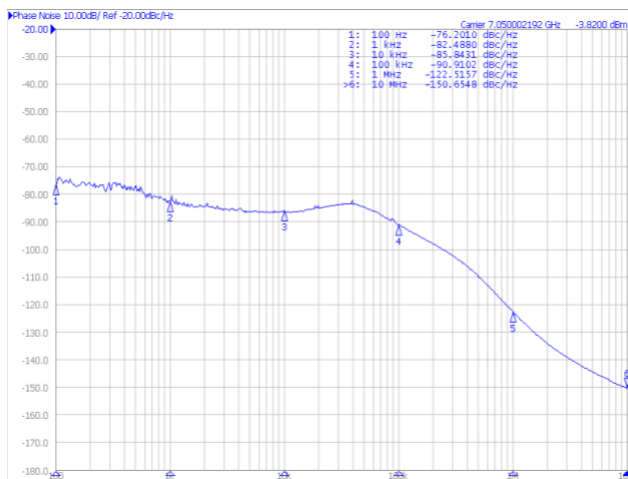


Figure 12. LO MCM output phase noise.

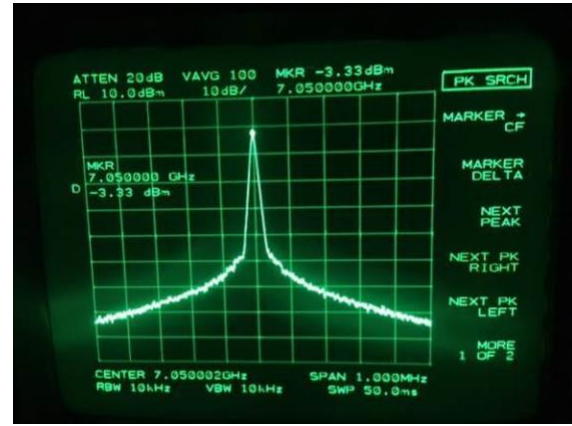


Figure 13. LO MCM output spectrum.

For reliability testing thus far, we have completed 200 thermal cycles from -55°C to 100°C with no noticeable degradation in RF or DC performance.

Current and Future Work

Tests remaining include RF measurements over temperature, more thermal cycling and radiation testing. In the near future the plan is to realize the remaining circuits from the Exciter and the Receiver in MCM form in order to further minimize the volume of the radio. The goal is to reduce the Exciter and Receiver subsystems from 2 boards down to 1 side of a board measuring 10cm by 10cm by 1cm. A long term goal for the radio is to put the power supply and the digital processor along with the RF electronics in 3D stackable MCMs that take up about 5cm by 5cm by 5cm or about 1/8th of a Cubesat Unit.

3. CERAMIC LEADLESS CHIP CARRIERS

Leadless Chip Carrier Technology Description

Ceramic leadless chip carriers have been used extensively throughout the aerospace, defense and commercial industries for decades. These packages are typically used to house high reliability ICs and recently can support frequencies up to and beyond 40GHz. The packages are typically made of Al₂O₃ or Alumina but for high power applications can be made of more exotic materials such as Aluminum Nitride (AlN) or Beryllium Oxide (BeO). For our RF electronics repackaging effort we currently have two parallel efforts which are ongoing in which we explore electronics miniaturization for low cost higher risk missions and then also for low risk higher cost applications.

Low Cost Repackaging Effort for Small Sats

The first effort is tailored for Cubesat applications in which we purchase high temperature co-fired ceramic (HTCC) packages from Barry Industries and use them to repack bare die which are typically offered in much larger packages. Figure 14 shows a comparison between a COTS

package on the left and the Barry Industries 6mm QFN on the right.

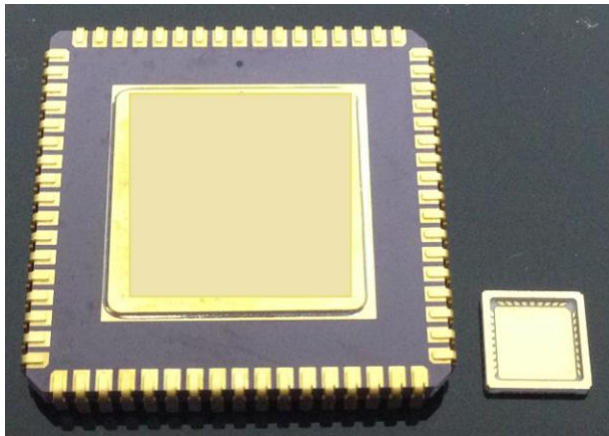


Figure 14. COTS IC package 24mm on a side next to 6mm on a side Barry Industries HTCC unpopulated package which would carry the same die.

Figure 15 shows the populated 6mm square package without a cover in which a PLL die is mounted using a non-conductive epoxy and the small single layer capacitor is mounted using a conductive silver epoxy. The die is fabricated on a silicon on sapphire process selected for its radiation hardness characteristics. Overall, we get at least a ¼ reduction in board real estate when using these packages especially where we are repackaging die in which there are IO that we do not need.

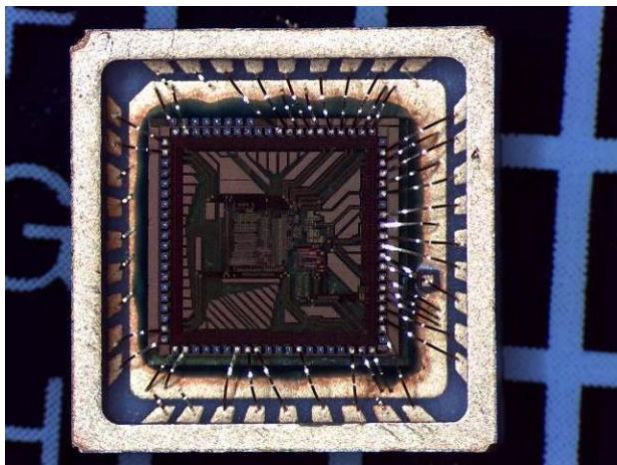


Figure 15. Rad hard die mounted in a 6mm square HTCC package from Barry Industries.

Due to the ease of use and availability of the packages, we have been able to use them extensively throughout current Cubesat projects. Figure 16 shows a snapshot of a board assembly in which we implement the use of 3 parts in a synthesizer circuit used on the Iris V2 radio which is planned to be launched on MarCO in 2016.

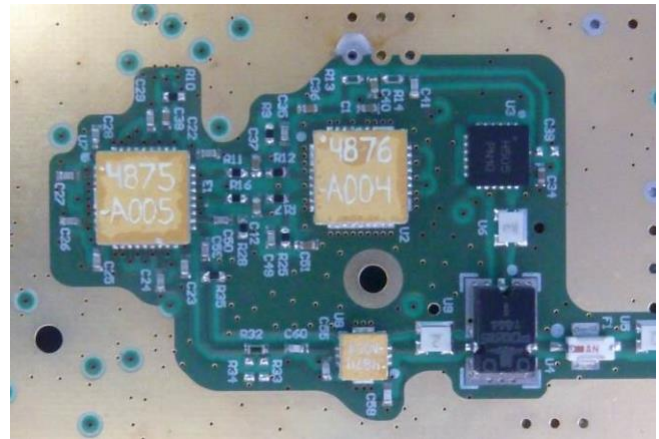


Figure 16. Portion of the Iris V2 Exciter board assembly in which 3 (gold with white lettering) custom Barry Industries packages are used to reduce the overall board routing area.

Another added benefit to designing in these packages has been the availability of test fixtures. We are currently evaluating various test fixtures from Ardent Concepts in which we are able to place assembled packages into socketed test fixtures prior to SMT attach on our board assemblies. This helps to assure that we have known good packaged parts that have been characterized before soldering them down. Figure 17 shows a photo of a custom test fixture from Ardent Concepts used for the 6mm square Barry Industries package.

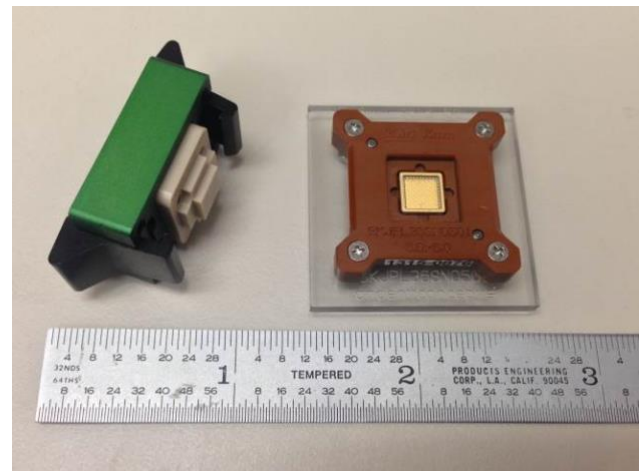


Figure 17. Custom test fixture from Ardent Concepts used to test packages prior to SMT attach to printed circuit board assemblies.

Repackaging Effort for High Reliability Missions

The second effort in this task addresses the need to reduce complexity in chassis fabrication and assembly for high reliability missions. With the recent advancement in packaging technologies at KCB Solutions, we have been able to partner with them to further evolve many of our higher frequency assemblies. KCB Solutions provides the packaging design and screening necessary to flight qualify

our assemblies for high reliability missions. The typical process is that we provide them with the part numbers of the devices we would like to package for SMT along with some performance specifications and they provide the design, final product hardware, screening and overall packaging expertise.

A couple of examples of this are shown in Figures 18 through 21. Figure 18 shows a MMIC amplifier that is typically mounted using hybrid assembly techniques in a complex chassis that has been repackaged into a high frequency hermetic ceramic package. The packaged device is designed to operate at 26GHz with greater than a 5GHz bandwidth. The package measures about 5mm on a side by about 1.4mm tall.

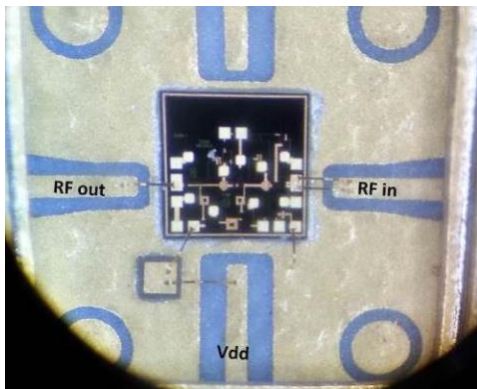


Figure 18. MMIC amplifier assembly mounted in a high reliability hermetic ceramic package from KCB Solutions [6].

Now that the device is mounted in a surface mount package, it can be easily tested and soldered to a custom evaluation board also courtesy of KCB solutions and shown in figure 19.

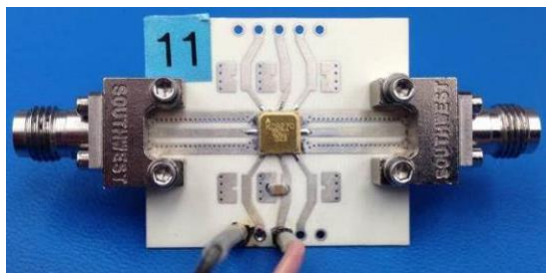


Figure 19. SMT packaged MMIC amplifier mounted to custom evaluation board.

In addition to single chip packages, KCB solutions is also providing us with a multichip module in a ceramic leadless package. This circuit is designed as a high rate modulator which integrates an IQ mixer, LO amplifier and RF amplifier. The LO input to this part is 13GHz, the RF output is centered at 26GHz and the IF input supports greater than 1GHz of bandwidth. This package measures about 5mm by 9.3mm by 1.4mm tall. Figure 20 shows the

internal package MMIC assembly and Figure 21 shows the package mounted to an evaluation board.

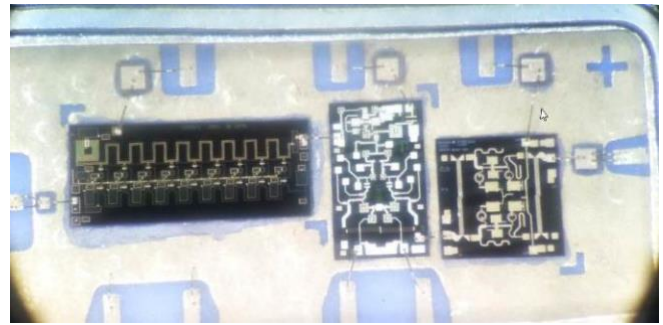


Figure 20. Multi-MMIC modulator assembly mounted in a custom high reliability hermetic ceramic package from KCB Solutions [6].

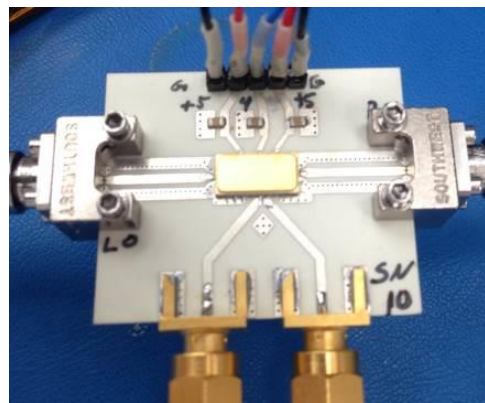


Figure 21. SMT packaged high rate modulator mounted to custom evaluation board.

Typically the MMICs used in these packages along with those in the previous example would need to be attached directly to the chassis floor in an isolated chip and wire cavity that would need to be kept separated from the SMT assemblies. With the high frequency hermetic SMT packaging now available, we can make use of various high frequency devices in SMT assemblies. This in turn reduces our overall chassis mass and complexity. Careful attention still needs to be taken in order to assure cavity modes and crosstalk doesn't exist on the printed circuit board assembly but this issue has been largely addressed with internal covers and RF PCB layout methods [7].

4. 3D PRINTED WAVEGUIDE DIPLEXER

Task Description

The additive machining process as applied to waveguide structures has been in use for more than 5 years. The intent of this task was not to perform research in the additive machining processes but more so to develop a method for realizing complex waveguide structures in a process that can be flown in the near term on Cubesat platforms. A waveguide diplexer is the component that was selected due

to its high CNC machining cost and complexity along with its frequent use for interconnecting our radios to the antenna in full duplex Ka-Band applications. The preference has historically been to machine our diplexers for reasons including machining tolerance accuracy and low loss smooth metallic finish. We explored a few technologies to replace this CNC process in order to reduce the cost and delivery time of machining, for cases where rapid prototyping is required and where specifications may be relaxed enough to handle the additional RF losses.

Waveguide Diplexer Design Method

The diplexer requirements are shown in table 1. It is designed to be frequency compatible with the deep space network (DSN) Ka band.

Ka-Band Diplexer Requirements	
Transmit Frequency	31.8-32.3GHz
Receive Frequency	34.2-34.7GHz
Insertion loss in-band	<1dB
Isolation	>60dB
Return loss in-band	>10dB

Table 1. DSN Ka-Band diplexer requirements.

The design process for the Ka-Band waveguide diplexer is as follows:

1. Use WaspNet [8] for synthesizing an E-plane bifurcated tee with iris band pass filters.
2. Verify design in HFSS [9] and if necessary iterate the design in WaspNet to optimize the performance.
3. Add in waveguide bends and add in radii and chamfers where applicable and verify again in HFSS.
4. Build model for machining.

The WaspNet EM software is a hybrid mode matching simulator which allows for a rapid synthesis of waveguide structures. A snapshot of the WaspNet simulation results is shown in figure 22.

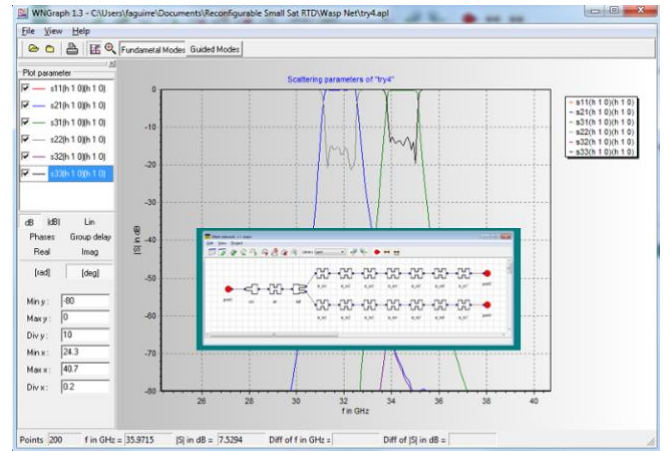


Figure 22. WaspNet simulation results for Ka-Band diplexer synthesis.

The HFSS simulation model with the 34GHz field distribution are shown in Figure 23.

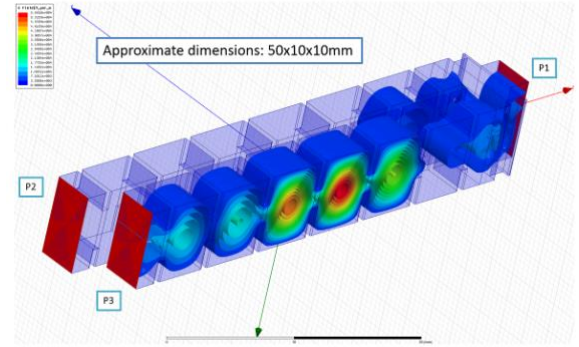


Figure 23. HFSS model of diplexer with electric fields plotted at 34GHz and shown here for a relative field intensity view.

The HFSS simulation results are shown in figure 24. The simulation results met all of the requirements in table 1.

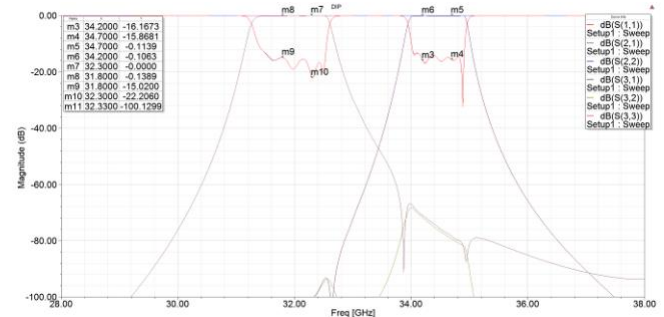


Figure 24. HFSS simulation results of diplexer.

3D Printed Waveguide Diplexer Fab and Test Results

Direct metal laser sintering (DMLS) was the first process selected to realize the waveguide diplexer. DMLS is as the name implies, a laser sintering process that uses $\text{AlSi}_{10}\text{Mg}$ as its base powder metal [10]. The final material lends itself to post processing for purposes of improving surface roughness and thermal conductivity [11]. For reducing surface roughness and tensile stresses, we typically finish all surfaces using micro shot-peening which is similar to a sand blasting process [12]. In addition to shot-peening, critical contact surfaces are also manually lapped. In order to increase the thermal conductivity of the metal after sintering, we also put the hardware through a hot isostatic pressing (HIP) process which removes the porosity of the material [13]. The company which we selected for our DMLS fabrication and support was Forecast 3D [10].

The waveguide assembly for the initial design was for a split block construction. The waveguide was cut at its center in the max E-field across the H-Plane where the current and fields are least sensitive to discontinuities in the chassis [14]. Figure 25 shows a photo of the split block diplexer opened up (left) and on the test bench (right).

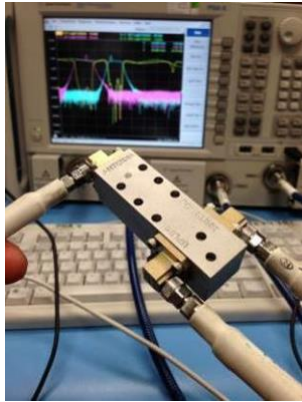


Figure 25. DMLS Ka-band split block diplexer opened up (left) and on the test bench (right).

The test results of the DMLS diplexer are shown in figure 26, 27 and 28.

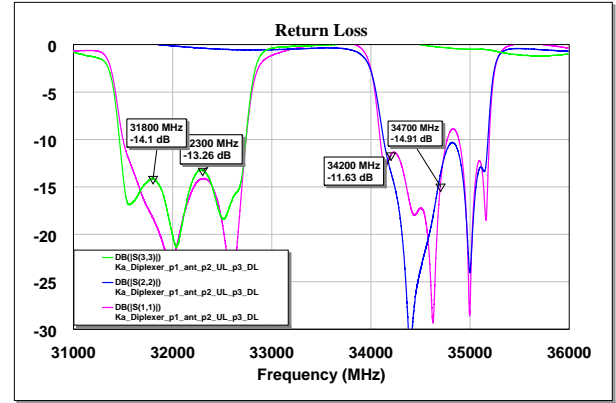


Figure 26. Return loss test results of diplexer.

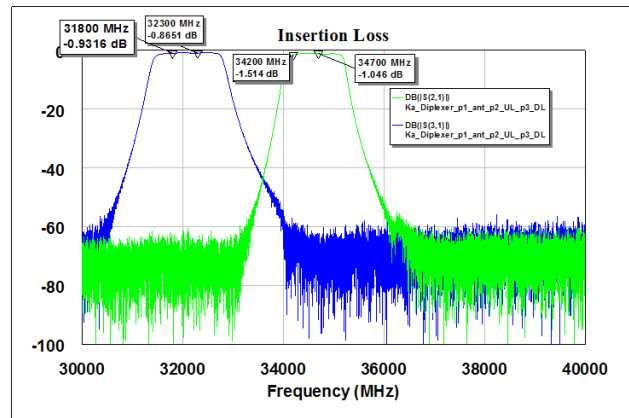


Figure 27. Insertion loss test results of diplexer.

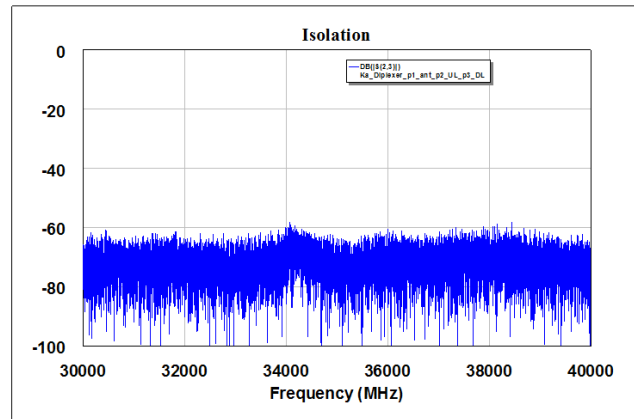


Figure 28. Isolation test results of the diplexer.

The RF performance of the DMLS version of the diplexer is acceptable for some of our lower power small satellite applications. The insertion loss of the uplink passband was slightly higher than expected but even with this, DMLS shows promise for rapid prototyping. Overall, the cost and schedule were about $1/10^{\text{th}}$ that of the CNC version quote for the same diplexer model.

Work that is currently in progress for additive machining includes hardware composed of metal plated plastic polymer technology from Swissto12 [15]. We are currently testing and optimizing our hardware samples of which a photograph is shown in figure 29.

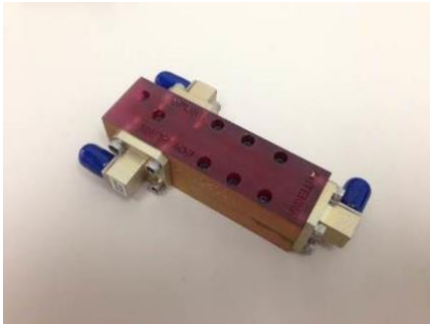


Figure 29. Photo of the fully assembled metal plated plastic 3D printed diplexer (top) and the same diplexer disassembled to open face view.

5. SUMMARY

We have presented 3 different examples of electronic packaging miniaturization methods that show potential for application in small spacecraft. The first example of the organic MCM allowed us to make a reduction in routing area of almost $1/10^{\text{th}}$ compared to using the COTS available packaging. We performed 200 thermal cycles from -55°C to 100°C and saw no noticeable degradation in electrical performance. Our second example implemented the use of more traditional ceramic packaging methods as applied to both lower risk high cost missions and higher risk low cost missions. Once again in this example, we saw a major reduction in routing real estate close to about $1/4^{\text{th}}$ as compared to using the standard flight packages. Our final example was that of an additive machined Ka band waveguide diplexer. We described both the DMLS and a metal coated plastic process. The DMLS is currently

furthest along and shows greater than 60dB of isolation between transmit and receive frequencies for the Ka-Band DSN deep space bands.

For all of the packaging technologies described, our original intent was to find and implement packaging technologies that could be applied today or in the near future. Based on the performance results, we believe that our intent was met. That being said, as with any new technology when applied in high reliability applications, there are numerous screening tests that still need to be performed. We plan to run more thermal cycles and outgassing tests for all of the hardware along with radiation testing where applicable. If any of these results are available at the time of the conference, they will be presented then.

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Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

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BIOGRAPHY



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